1. (Amended) A circuit, comprising a comparator having an output and a pair of inputs, wherein the pair of inputs are adapted to receive an output signal produced from the circuit and a reference voltage forwarded to the circuit, and wherein the circuit further comprises:

a pull-down transistor connected to one of the pair of inputs and the output; and

a pull-up transistor coupled between a power supply and said one pair of inputs.

4. (Amended) The circuit as recited in claim 1, wherein the pull-down transistor comprises a gate conductor and a source-to-drain current path between said one of the pair of inputs and a ground supply voltage whenever a voltage of the output coupled to the gate conductor exceeds the reference voltage.

6. (Amended) The circuit as recited in claim 1, wherein the pull-up transistor comprises a gate conductor and a source-to-drain current path between the power supply voltage and said one of the pair of inputs whenever a voltage of an input signal coupled to the gate conductor exceeds a voltage of the output signal by a threshold voltage of the pull-up transistor.

7. (Amended) A system for adjusting a pulse width of an output signal, comprising:

a circuit for maintaining a reference voltage between a positive and negative voltage peaks of the output signal;

a comparator coupled to compare a voltage of the output signal to the reference voltage; and

a pull-down transistor coupled to an output of the comparator for fixing a minimum voltage of the output signal to a voltage approximately equal to the reference voltage whereby the pulse width of the output signal varies in proportion to changes in the reference voltage.

11. (Amended) The system as recited in claim 7, wherein portions of the output signal below the reference voltage are chopped and remove at the reference voltage.

12. (Amended) The system as recited in claim 7, wherein the comparator comprises a slew rate and/or gain, and which is predetermined to preclude a voltage of the output signal from being less than the reference voltage.

13. (Amended) The system as recited in claim 7, wherein the pull-down transistor comprises a gate conductor and a source-to-drain current path, wherein the gate conductor is coupled to receive an output from the comparator and the source-to-drain current path is maintained during times when the reference voltage is maintained at approximately a midline voltage between the positive and negative voltage peaks of the output signal.

16. (Amended) A method for regulating a duty cycle of an output signal, comprising presenting the output signal into a comparator for comparing the output signal to a predetermined reference voltage and feeding back the results of the comparison to a pull-down transistor that chops the output signal between a periodic and symmetric positive peak voltage value and the reference voltage, whereby the time at which the positive peak voltage value extends above the reference voltage is directly proportional to the duty cycle of the output signal.

17. (Amended) The method as recited in claim 16, wherein said presenting comprises connecting a positive input of the comparator to a conductor that receives the output signal and connecting a negative input of the comparator to a conductor that receives the reference voltage.

18. (Amended) The method as recited in claim 16, wherein said feeding back comprises forwarding a voltage which remains above a threshold voltage of the pull-down transistor, from the comparator to a gate conductor of the pull-down transistor to ensure the pull-down transistor is always active.

19. (Amended) The method as recited in claim 16, wherein said feeding back comprises chopping a negative-going waveform of the output signal at a level of the reference voltage, and wherein varying the level of the reference voltage changes the pulse width and duty cycle of the output signal.